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ECE 422

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Phase Shift Network Design

# Introduction

**\* Note: for final report Continue to pg.5**

The specifications for this Network included.

* Analyze network on paper.
* Redesign to run off a 3V supply, with a current draw of less than mA
* Gain of 0dB for pass, and gain of -40dB for rejection.
* Bandwidth of 300 Hz – 3K Hz.

Approaching this design I had to get a better understanding of what the phase shift network did and what the output should look like, in theory the network is a type of analog filter that takes two inputs I and Q which are 90° in phase or out, and based on that phase either passes the signal through or rejects them, to get a visual ideal of this I simulated the given circuit in class, The circuit runs on a 6V supply and is capable of rejection around 37dB.

After getting a better Idea of what the circuit behaves like, I began by examining the topology of the circuit and was able to recognize an amplifier and output stage, but the in between network was not familiar; this must be where the magic happens.

I began analyzing an individual input since both I and Q circuits were both identical except for the phase shift network portion, I solved for the dc currents and voltages and compared them to what Ltspice output, which were fairly close.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Gain Stage | | Output stage | |
|  | Ltspice | Calculated | Ltspice | Calculated |
| Ic | 11.6mA | 11.8mA | .31mA | .29mA |
| Ib | 39.8uA | 39.4uA | .99uA | .9uA |
| Vbe | 1.88V | 2.14V | 2.07V | 2.14V |
| Vc | 1.76V | 1.67V | 6V | 6V |
| Ve | 1.16 | 1.19 | 1.45V | 1.37V |

Table 1 – Calculated Dc values vs Ltspice

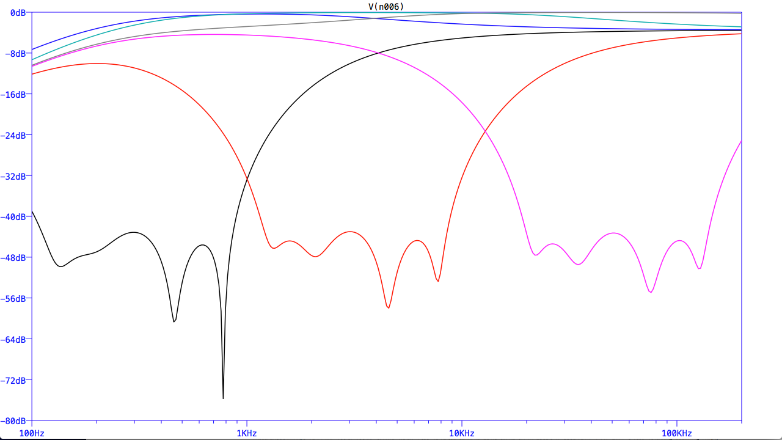
In the Ac analyze I was able to calculate the small signal parameters, but in trying to understand the frequency response of the circuit and how the pass and rejection worked just ended in frustration, so I decided to work on the redesign. I first played around with the original circuit and varied various component values to get an understanding of how the circuit behaved, I found that if you scale all the capacitors in both phase networks you can shift the bandwidth of the rejection around, I also found that varying the betas of the transistors from 50 to 500 did not have a significant difference.

Figure 1 - scaled Capacitors

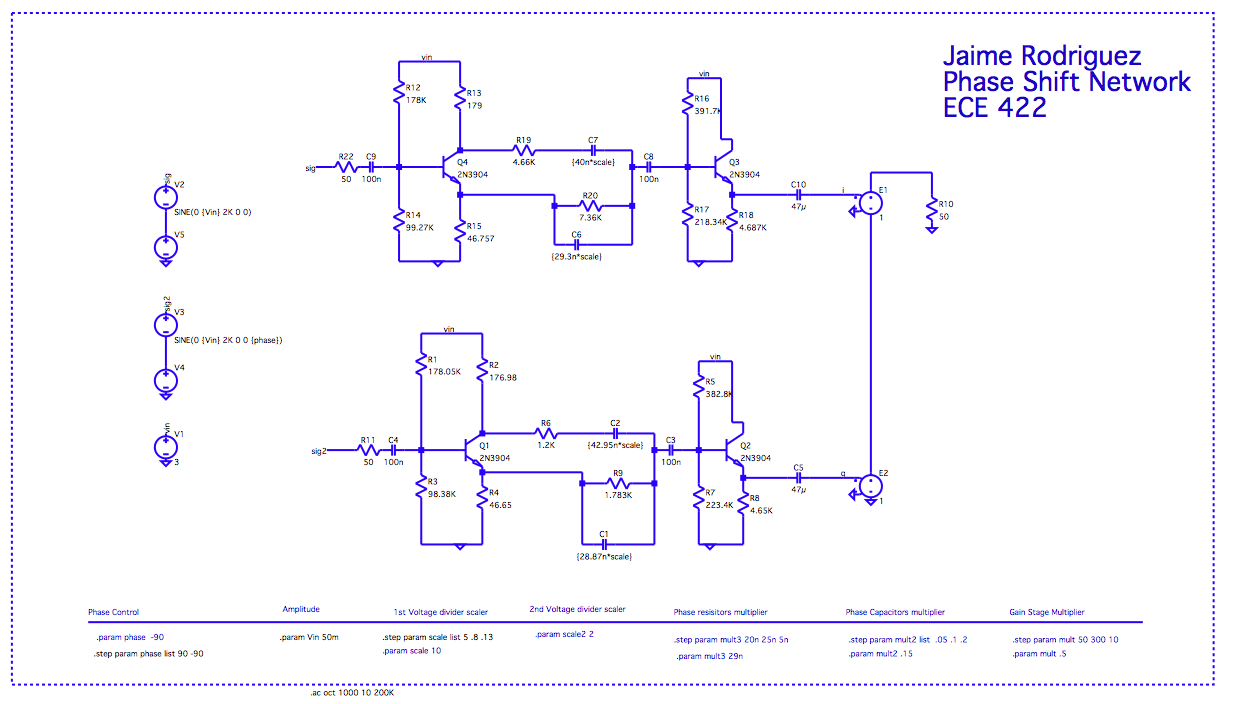
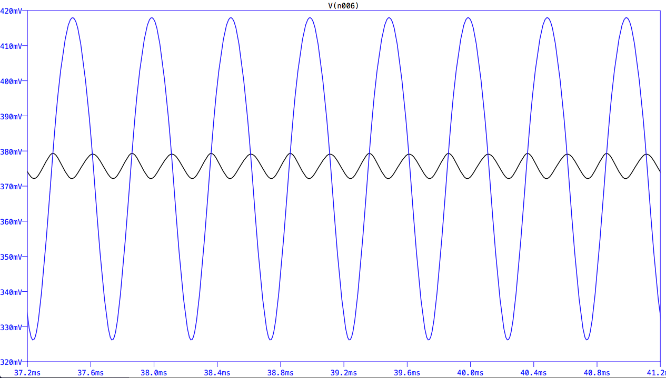
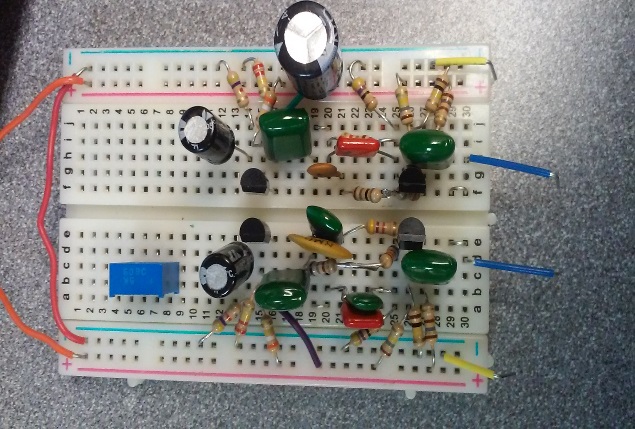


Figure 2 - Redesigned Circuit

Figure 3 - Screen shot of transient

 In my redesigned circuit above, I basically lowered the voltage to 3V and just played around scaling values until I found something that worked relatively well to the required specifications. I ended up with a circuit that had a passband of around 0 dB with a rejection of -44dB at the highest and -66db at the lowest and a bandwidth of 400Hz to 4 KHz, the total current draw is about 1.47mA.



I was happy enough with the design so I went ahead and built the circuit, on my first attempt at prototyping turned out unsuccessful, this was because I chose values that just close to what I used in spice, so I spent some time measuring my resistors, capacitors and reworking my design to fit what I had in my tool box. After having matched all my components to be as close to the values in my simulation I setup my circuit and took measurements at various frequencies having the Q input in and out of 90° phase, the measured values are in the table below.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Frequency (Hz)** | **Vin (mV)** | **(90° mV)** | **Gain (dB)** | **(-90°mV)** | **Gain (dB)** |
| 10 | 48 | 17 | -9.3704217 | 18 | -8.87395 |
| 40 | 48 | 16 | -9.8970004 | 32 | -3.8764005 |
| 100 | 48 | 14 | -11.056839 | 36 | -2.8533501 |
| 200 | 48 | 10 | -13.9794 | 48 | -0.3545753 |
| 300 | 48 | 4 | -21.9382 | 54 | 0.66847511 |
| 400 | 48 | 1 | -33.9794 | 58 | 1.28915978 |
| 500 | 48 | 0.8 | -35.9176 | 60 | 1.58362492 |
| 600 | 48 | 0.8 | -35.9176 | 60 | 1.58362492 |
| 700 | 48 | 0.8 | -35.9176 | 60 | 1.58362492 |
| 800 | 48 | 0.8 | -35.9176 | 60 | 1.58362492 |
| 900 | 48 | 0.8 | -35.9176 | 60 | 1.58362492 |
| 1000 | 48 | 0.8 | -35.9176 | 62 | 1.8684337 |
| 2000 | 48 | 0.8 | -35.9176 | 61 | 1.72719661 |
| 3000 | 48 | 0.8 | -35.9176 | 61 | 1.72719661 |
| 4000 | 48 | 0.8 | -35.9176 | 61 | 1.72719661 |
| 5000 | 48 | 0.8 | -35.9176 | 61 | 1.72719661 |
| 6000 | 48 | 1.6 | -29.897 | 60.8 | 1.6986715 |
| 7000 | 48 | 14 | -11.056839 | 60 | 1.58362492 |
| 8000 | 48 | 16 | -9.8970004 | 60 | 1.58362492 |
| 9000 | 48 | 19.5 | -8.1787079 | 59 | 1.43764015 |
| 10000 | 48 | 20 | -7.9588002 | 59 | 1.43764015 |
| 20000 | 48 | 33 | -3.6091213 | 55 | 0.8278537 |
| 30000 | 48 | 37 | -2.6153656 | 52 | 0.34066679 |
| 40000 | 48 | 39 | -2.1581079 | 50 | 0 |
| 50000 | 48 | 40 | -1.9382003 | 48 | -0.3545753 |
| 60000 | 48 | 39 | -2.1581079 | 48 | -0.3545753 |
| 70000 | 48 | 38 | -2.3837282 | 47 | -0.5374429 |
| 80000 | 48 | 39 | -2.1581079 | 46 | -0.7242435 |
| 90000 | 48 | 39 | -2.1581079 | 45 | -0.9151498 |
| 100000 | 48 | 38 | -2.3837282 | 45 | -0.9151498 |

Figure 4 - Prototype

Table 2 – Measured Values

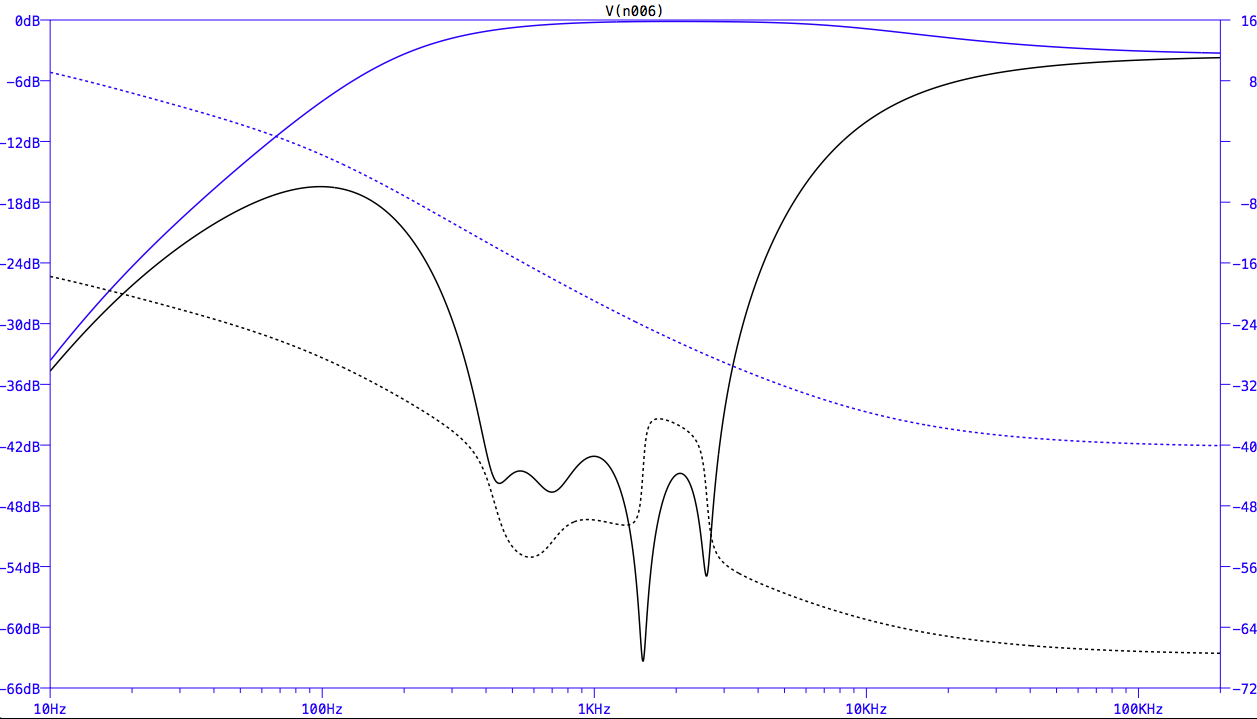


Figure 5 – Simulated frequency response

Figure 6 - Plot of measured Values

# Final Report (91.5MHz Receiver)

From early on in this class I was very interested in building a receiver of my own and I now believe that I am at a point where I can accomplish this, in my previous report I stated that I wanted to just focus on the phase shift network which I’ve built and tested showing very similar results to what I was receiving in simulation with a rejection of around -38dB and running with a current draw of 2.4mA a little over spec, but instead of continuing work on this I decided to switch gears and build a FM radio with a band of 80MHZ to 110MHZ with same power requirement of 3V as in the phase shift network, in the block diagram below I’ve outlined the major components in the radio and the progress that I’ve made so far.



Figure 7 - Current receiver progress

I first began this project by designing a 50 ohm input amplifier for the phase shift network created earlier, in simulation the design has the same response as before but with a gain of 25dB, the input resistance is also measured to be around the 50ohm mark, I have not yet built the design.

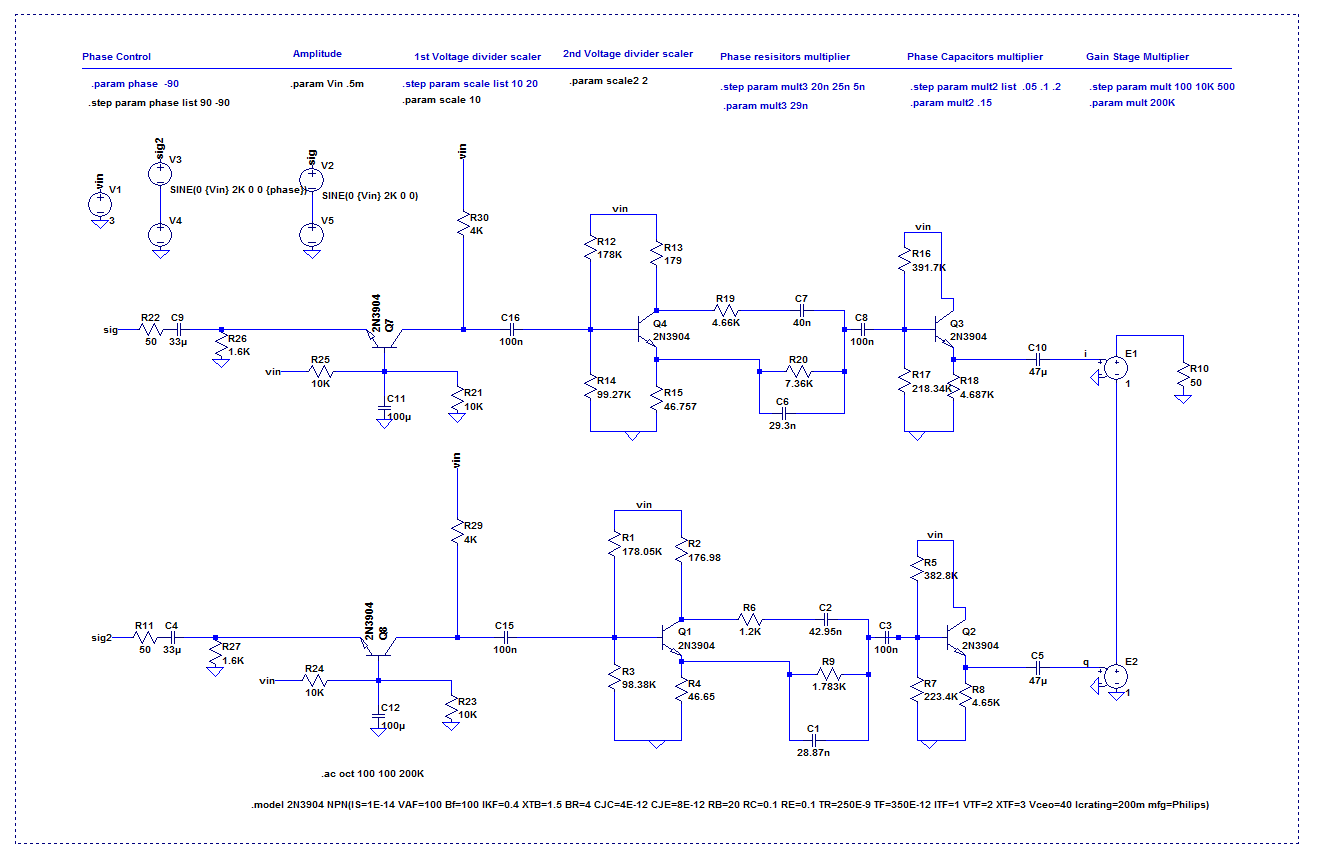
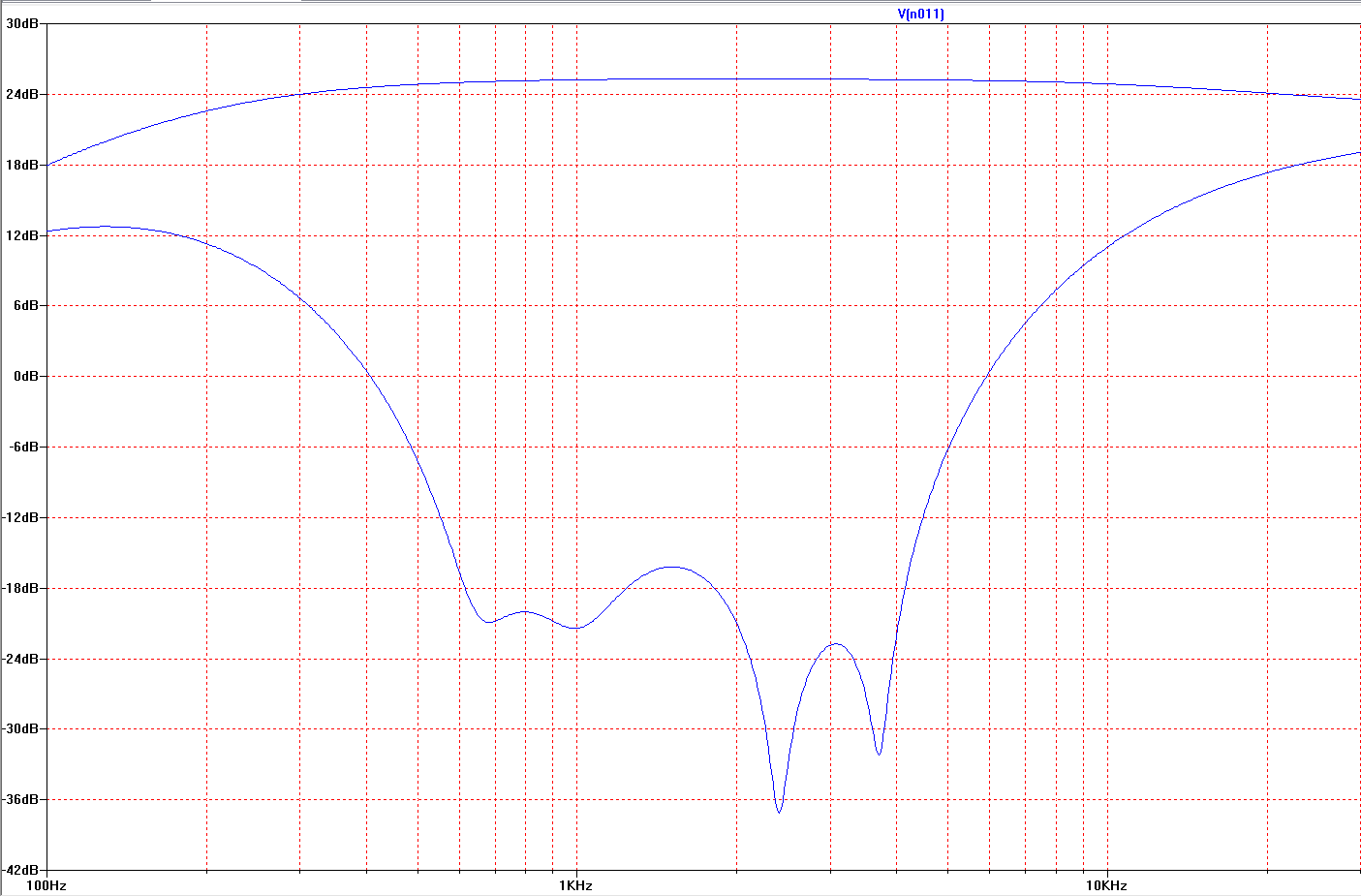


Figure 8 - Phase shift with LNA

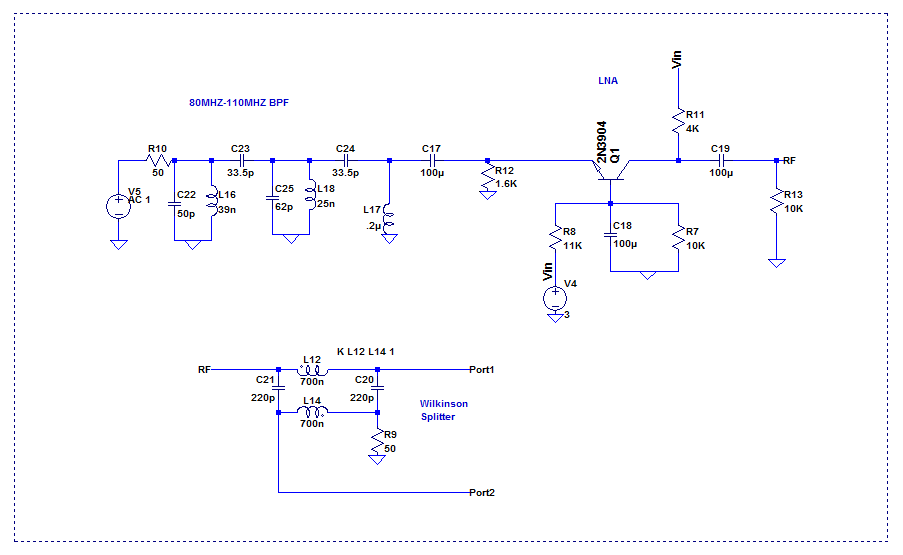
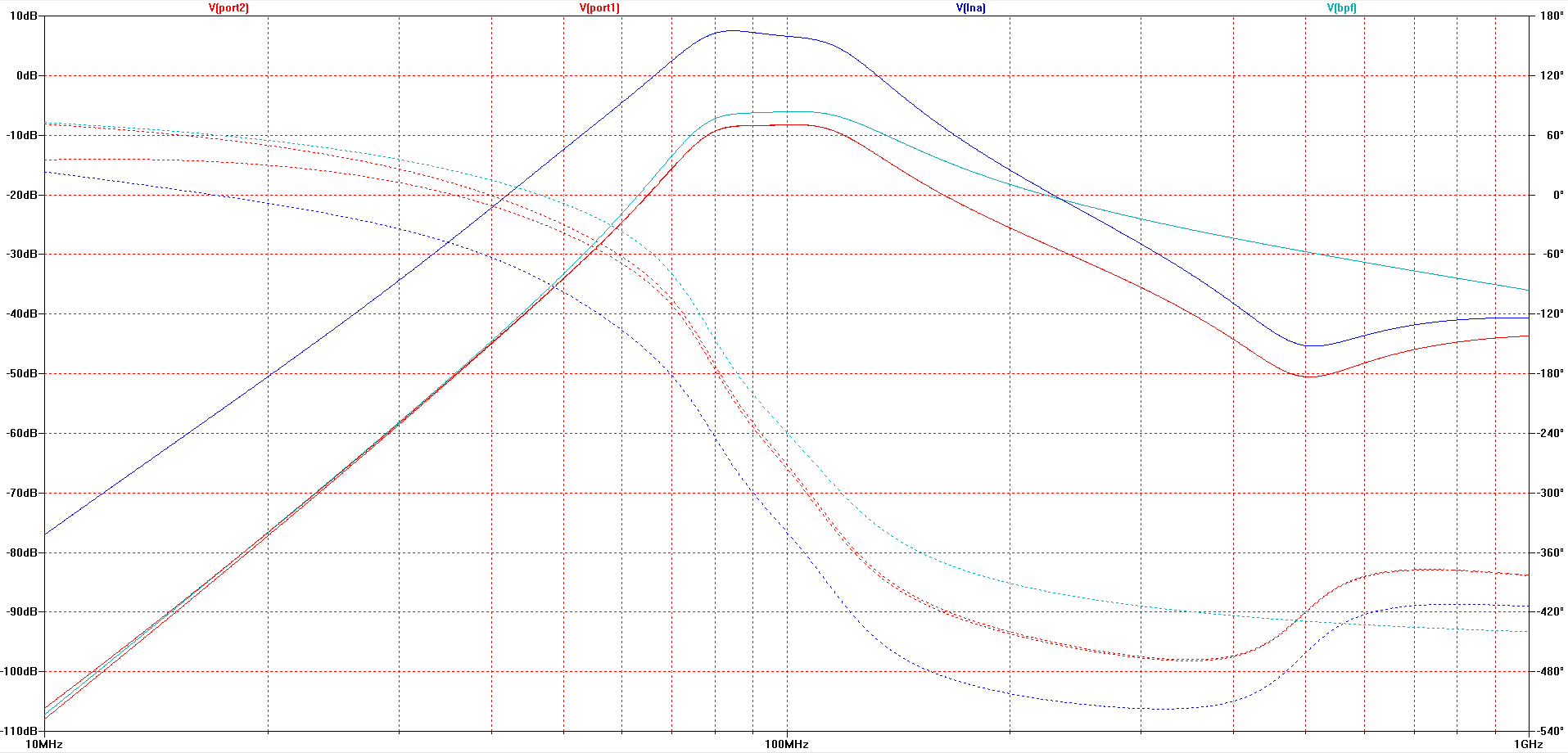


Figure 9 - BPF & LNA into splitter

I’ve also started designing the bandpass filter for the raw RF signal, this design was created using the technique described in lecture of starting with a prototype lowpass filter and then transforming into a bandpass, the component values where then scaled up, the final filter in the circuit shown was obtained after adding quarter wave transformers and just playing around with the values. In simulation I’ve also added a 50ohm amplifier with a Wilkinson splitter just for testing. I am still unsure how much gain is need at this stage of the circuit.

Figure 10 - BPF,LNA and splitter



Conclusion:

The next part of the receiver that I will begin working on is the Local Oscillator, I haven’t taken ECE 323 yet so I’m not very familiar with the circuit but I am currently in the middle of building the VFO circuit seen down below so I can test and measure. I will also take ECE 323 next term so hopefully if I don’t finish designing my radio before then I can you use that class for improving my radio design, for the last stage of the receiver I will use my amp design which I created last term in 422 to drive the circuit, the amplifier was a 3 watt amp common emitter gain and a push pull output stage.

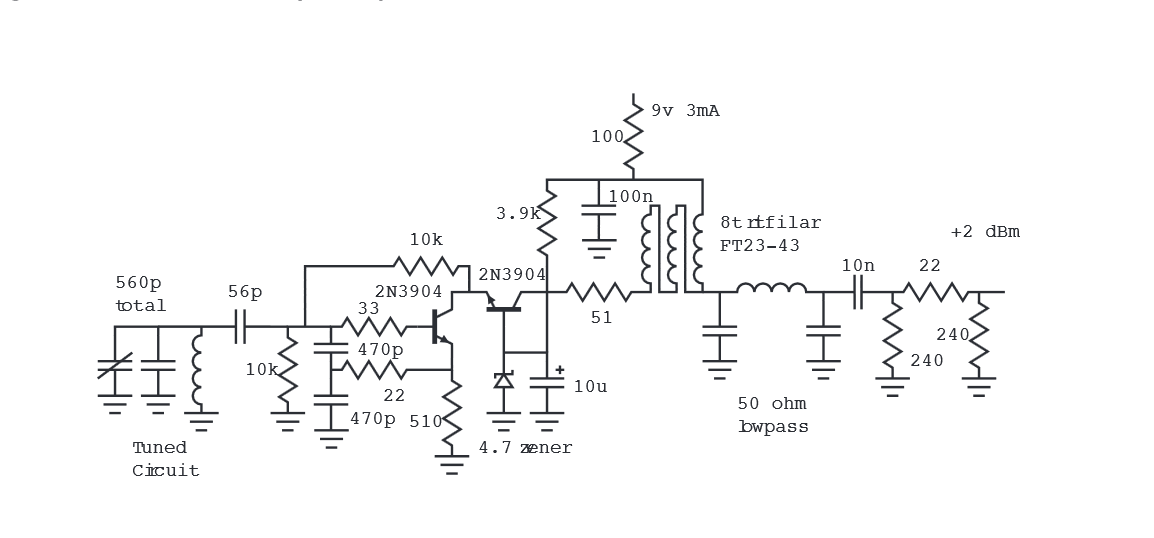


Figure 11 - Variable frequency oscillator